Fig.1

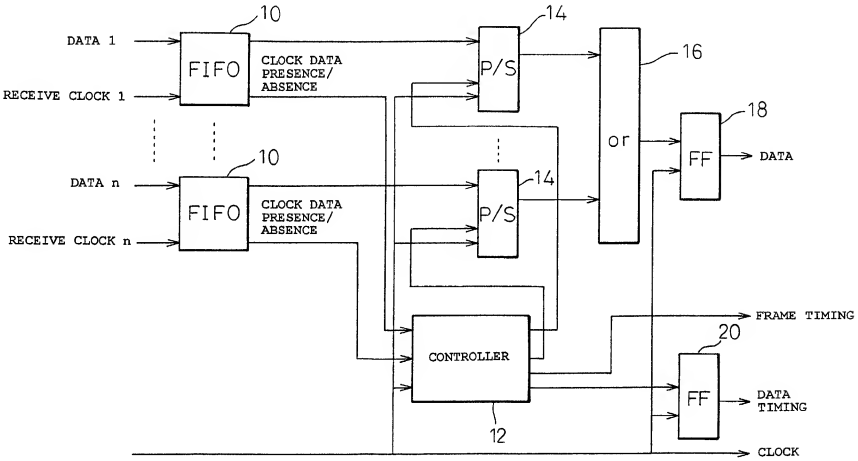

DATA 1
RECEIVE CLOCK 1
FIFO
10
CLOCK DATA PRESENCE/ ABSENCE
DATA n
RECEIVE CLOCK n
P/S
14
or
16
FF
18
DATA
CONTROLLER
12
FRAME TIMING
20
DATA TIMING
CLOCK

Fig.2

FIFO STATUS	DATA PRESENCE		DATA ABSENCE	
	FIRST BIT	SECOND BIT	FIRST BIT	SECOND BIT
DATA	1(0)	1(0)	×	×
DATA TIMING	0	1	0	0

Fig.3

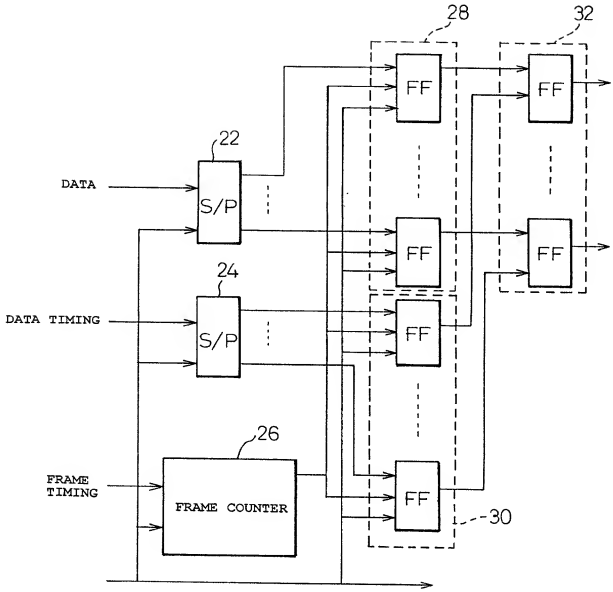

28
32
22
DATA
S/P
FF
FF
FF
FF
24
DATA TIMING
S/P
FF
26
FRAME TIMING
FRAME COUNTER
FF
30

Fig.4

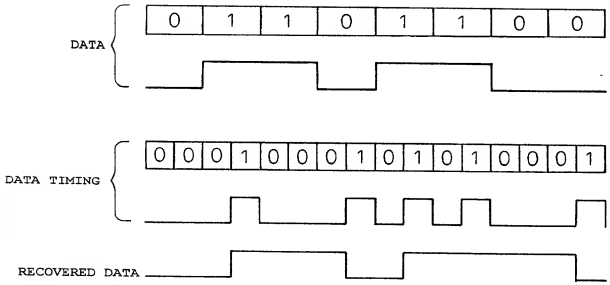
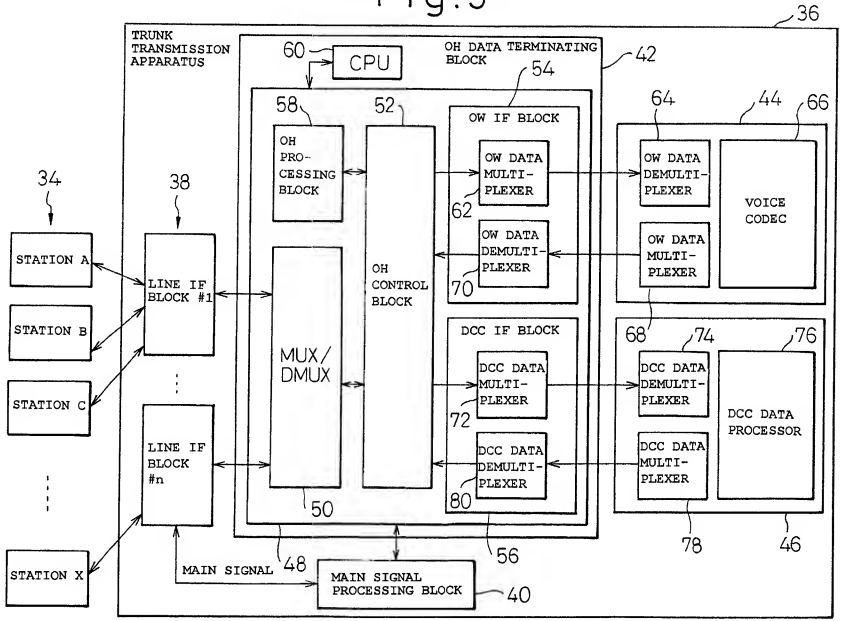
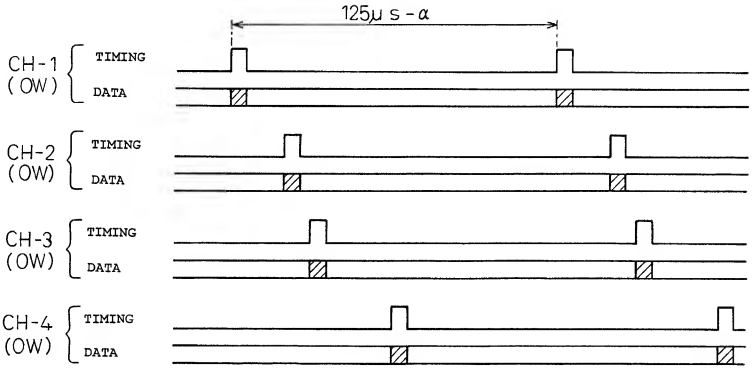

DATA
0 1 1 0 1 1 0 0
DATA TIMING
0 0 0 1 0 0 0 1 0 1 0 1 0 0 0 1
RECOVERED DATA

Fig.5


TRUNK TRANSMISSION APPARATUS
36
CPU
60
OH DATA TERMINATING BLOCK
42
54
58
52
OW IF BLOCK
64
44
66
OH PRO-CESSING BLOCK
OW DATA MULTI-PLEXER
OW DATA DEMULTI-PLEXER
VOICE CODEC
62
OW DATA DEMULTI-PLEXER
OW DATA MULTI-PLEXER
70
34
38
STATION A
LINE IF BLOCK #1
OH CONTROL BLOCK
STATION B
MUX/ DMUX
DCC IF BLOCK
68
74
76
STATION C
DCC DATA MULTI-PLEXER
DCC DATA DEMULTI-PLEXER
DCC DATA PROCESSOR
72
LINE IF BLOCK #n
DCC DATA DEMULTI-PLEXER
DCC DATA MULTI-PLEXER
80
50
STATION X
MAIN SIGNAL
48
56
78
46
MAIN SIGNAL PROCESSING BLOCK
40

3DST3D'CS8S/00T

Fig.6



20ET30"ES8S700T

Fig. 7

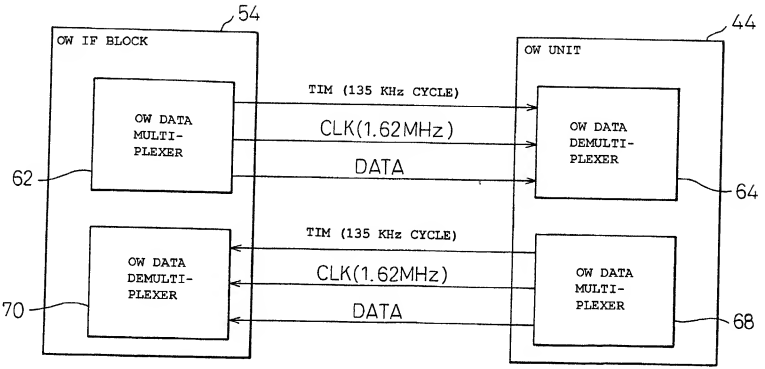


Fig.8

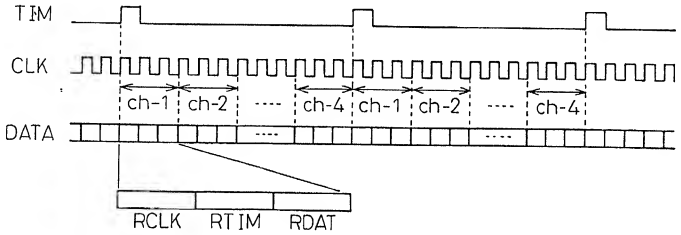


Fig.9

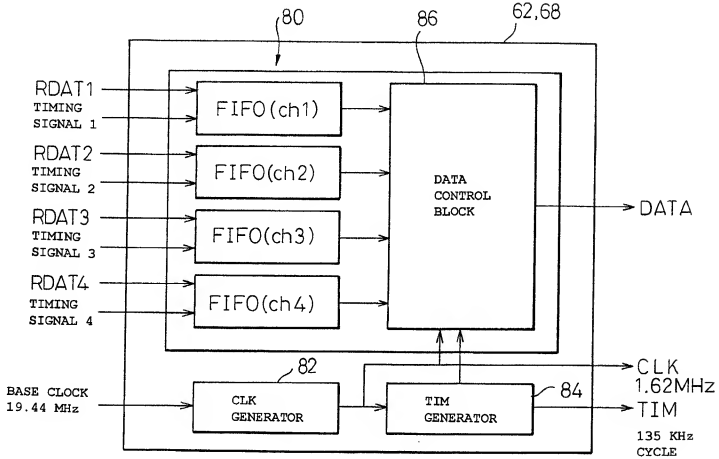

80
86
62,68
RDAT1
TIMING
SIGNAL 1
RDAT2
TIMING
SIGNAL 2
RDAT3
TIMING
SIGNAL 3
RDAT4
TIMING
SIGNAL 4
FIFO(ch1)
FIFO(ch2)
FIFO(ch3)
FIFO(ch4)
DATA
CONTROL
BLOCK
DATA
82
CLK
1.62MHz
BASE CLOCK
19.44 MHz
CLK
GENERATOR
TIM
GENERATOR
84
TIM
135 KHz
CYCLE

Fig.10

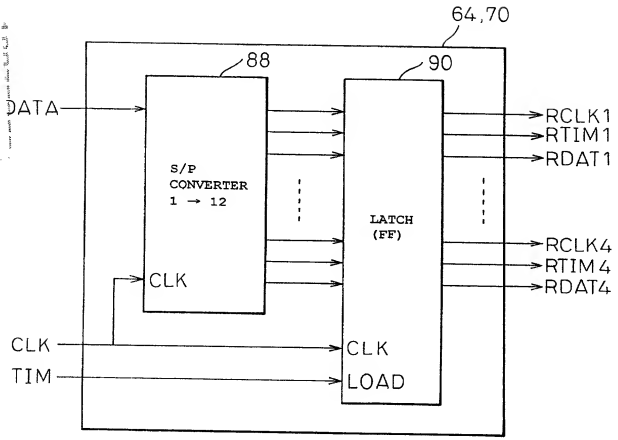

64,70
88
90
DATA
S/P
CONVERTER
1 → 12
CLK
LATCH
(FF)
RCLK1
RTIM1
RDAT1
RCLK4
RTIM4
RDAT4
CLK
TIM
CLK
LOAD

Fig.11

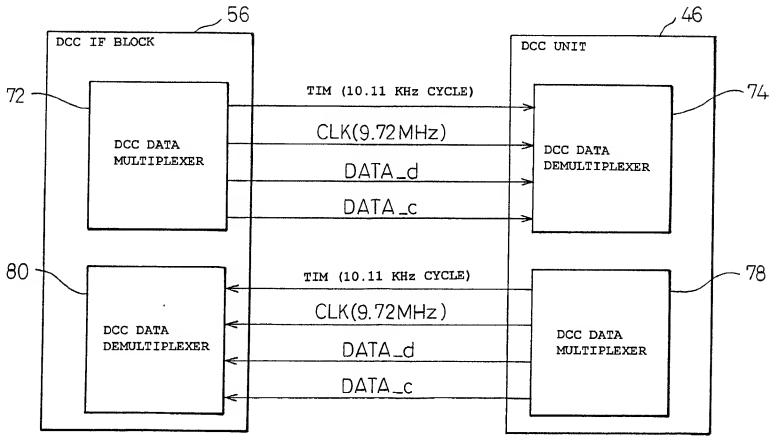

56
DCC IF BLOCK
46
DCC UNIT
72
DCC DATA MULTIPLEXER
TIM (10.11 KHz CYCLE)
CLK(9.72MHz)
DATA_d
DATA_c
DCC DATA DEMULTIPLEXER
74
80
DCC DATA DEMULTIPLEXER
TIM (10.11 KHz CYCLE)
CLK(9.72MHz)
DATA_d
DATA_c
DCC DATA MULTIPLEXER
78

Fig.12

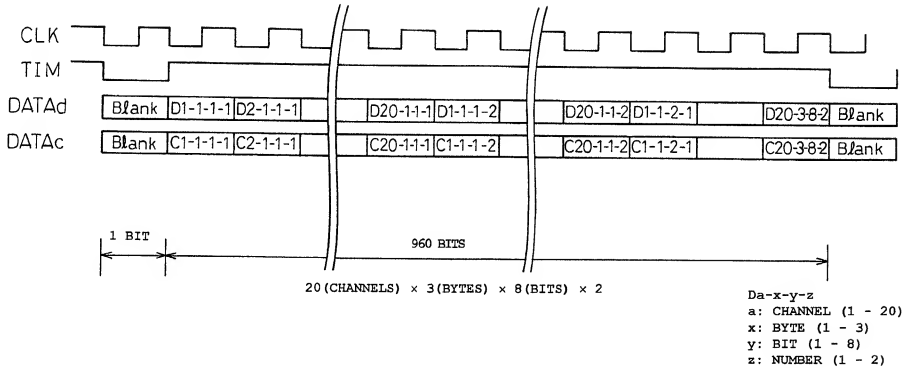

CLK
TIM
DATAd
DATAc
Blank
D1-1-1-1
D2-1-1-1
D20-1-1-1
D1-1-1-2
D20-1-1-2
D1-1-2-1
D20-3-8-2
C1-1-1-1
C2-1-1-1
C20-1-1-1
C1-1-1-2
C20-1-1-2
C1-1-2-1
C20-3-8-2
1 BIT
960 BITS
20(CHANNELS) × 3(BYTES) × 8(BITS) × 2
Da-x-y-z
a: CHANNEL (1 - 20)
x: BYTE (1 - 3)
y: BIT (1 - 8)
z: NUMBER (1 - 2)

Fig.13

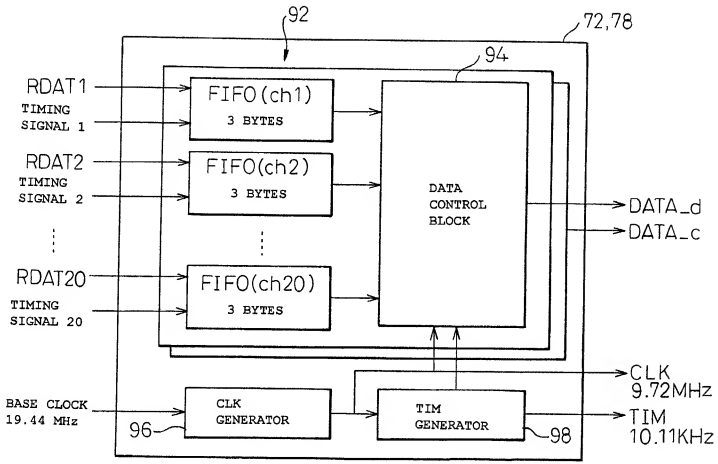
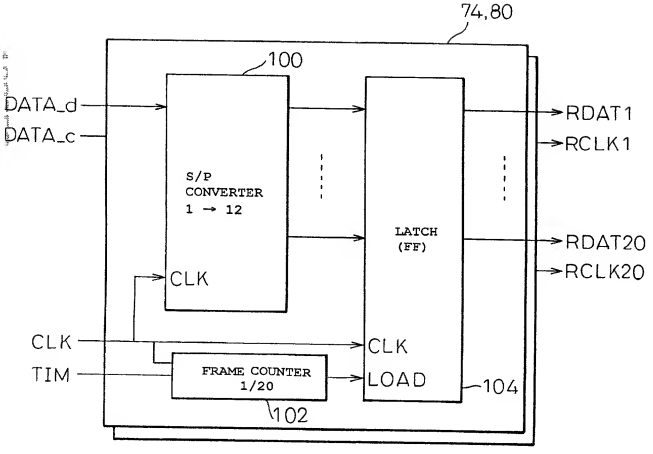

92
72,78
94
RDAT1
TIMING SIGNAL 1
FIFO(ch1)
3 BYTES
RDAT2
TIMING SIGNAL 2
FIFO(ch2)
3 BYTES
RDAT20
TIMING SIGNAL 20
FIFO(ch20)
3 BYTES
DATA CONTROL BLOCK
DATA_d
DATA_c
CLK
9.72MHz
TIM
10.11KHz
BASE CLOCK
19.44 MHz
CLK GENERATOR
TIM GENERATOR
96
98

Fig.14


74,80
100
DATA_d
DATA_c
S/P
CONVERTER
1 → 12
CLK
LATCH
(FF)
RDAT1
RCLK1
RDAT20
RCLK20
CLK
TIM
FRAME COUNTER
1/20
CLK
LOAD
104
102